Withdrawal of the rejection of claim 2 under 35 U.S.C. §112, first paragraph, is respectfully requested.

II. Claim 1 Satisfies the Requirements Under 35 U.S.C. §112, second paragraph

The Office Action rejects claim 1 under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 1 is now amended to obviate the rejection. Withdrawal of the rejection of claim 1 under 35 U.S.C. §112, second paragraph, is respectfully requested.

III. Claims 1 and 2 Define Allowable Subject Matter

The Office Action rejects claims 1 and 2 under 35 U.S.C. §102(b) and under 35 U.S.C. §103(a) over JP A 6-132306 to Morosawa et al.; and claims 1 and 2 under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) over JP A 5-55582 to Yamazaki et al. These rejections are respectfully traversed.

Morosawa and Yamazaki do not teach, disclose or suggest "an effective doping concentration of the crystallized semiconductor layer figuring 1 x 10^{18} cm^{-3} or less and the crystallized semiconductor layer having the thickness of 9 nm to 135 nm," as recited in claim 1. For avoiding a diffusion of impurities from a substrate and improving a quality of transistor, the claimed invention recites the figure of the effective doping concentration (see the specification, page 14, line 25 - page 15, line 16).

Morosawa and Yamazaki do not teach, disclose or suggest "the underlevel protection layer, the gate insulator, and the interlevel insulator layer comprising a silicon oxide film and having a combined thickness of 2 μm or less," as recited in claim 2. These recited features prevent a substrate from cracking (see the specification, page 17, lines 6-35).

Instead, Morosawa et al. merely discloses a glass substrate covered with a silicon nitride thin film 2 covered with a silicon oxide thin film 3, which is then covered with a polysilicon thin film 5.

Likewise, Yamazaki et al. merely discloses that a silicon oxide is formed on the first silicon nitride film.

For at least these reasons, Morosawa et al. does not anticipate the subject matter of claims 1 and 2 under 35 U.S.C. §102(b), nor does Morosawa et al. render obvious claims 1 and 2 under 35 U.S.C. §103(a); and Yamazaki et al. does not anticipate claims 1 and 2 under 35 U.S.C. §102(b), nor does Yamazaki et al. render obvious claims 1 and 2 under 35 U.S.C. §103(a). Withdrawal of the rejections of claims 1 and 2 under 35 U.S.C. §102(b) and under 35 U.S.C. §103(a) over Morosawa et al.; and claims 1 and 2 under 35 U.S.C. §102(b) and under 35 U.S.C. §103(a) over Yamazaki et al. is respectfully requested.

IV. The Obviousness-Type Double Patenting Rejection is Obviated

The Office Action rejects claims 1 and 2 under the judicially created doctrine of obviousness-type double patenting over claims 1-12 of U.S. Patent No. 6,335,542 to Miyasaka. In response, a Terminal Disclaimer is attached herein to obviate the judicially created doctrine of obviousness-type double patenting rejection. Withdrawal of the rejection of claims 1 and 2 under the judicially created doctrine of obviousness-type double patenting over claims 1-12 of Miyasaka is respectfully requested.

V. Conclusion

For at least these reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is requested.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number set forth below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Richard J. Kim
Registration No. 48,360

JAO:RJK/mdw

Attachments:
Petition for Extension of Time
Appendix
Terminal Disclaimer

Date: January 15, 2003

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claim(s):

1. (Amended) A thin film semiconductor device, comprising:

a substrate;

an underlevel protection layer ~~comprising an insulating material, the underlevel protection layer being formed on at least a portion of the substrate~~ formed over the substrate and including a plurality of films, at least one of which includes a silicon oxide; and

a crystallized semiconductor layer in contact with the film including the silicon oxide, wherein the crystallized semiconductor layer forms an active layer of a transistor,

an effective doping concentration of the crystallized semiconductor layer figuring $1x\ 10^{18}\ cm^{-3}$ or less and the crystallized semiconductor layer having the thickness of 9 nm to 135 nm, which are to prevent the spread of depletion layers from being constrained at the interface between the crystallized semiconductor layer and the underlevel protection layer

~~a semiconductor film formed on the underlevel protection layer creating an underlevel protection film, the semiconductor film being an active layer of a transistor and having a thickness between about 9 nm and 135 nm, the underlevel protection film comprising a plurality of different films, and the implantation dose is $1 x 10^{18}$ cm^{-3} or less., a top layer of film and a second layer of film, and the top layer of the underlevel protection film being a silicon oxide film formed on the second layer of film~~.

2. (Amended) A thin film semiconductor device, comprising:

a ~~glass~~ substrate ~~of 300 mm x 300 mm or more~~;

an underlevel protection layer ~~comprising~~ including an insulating material, the underlevel protection layer being formed on at least a portion of the substrate; and

a field effect transistor having:

~~three silicon oxide semiconductor films formed as said underlevel protection layer,~~a semiconductor film on the underlevel protection layer;

a gate insulator layer formed on the semiconductor film,

a gate electrode formed on the gate insulator layer; and

an electrically insulating interlevel insulator layer formed over the gate electrode and between interconnects of said field effect transistor, ~~the thin film semiconductor device having a thickness that is a sum of thicknesses of~~ the underlevel protection layer, the gate insulator layer, and the interlevel insulator layer comprising a silicon oxide film and~~, and the thickness of the thin film semiconductor device being~~ having a combined thickness of about 2 μm or less.